REMARKS

The applicants note with appreciation the acknowledgement of the claim for priority under section 119 and the notice that all of the certified copies of the priority documents have been received.

The applicants acknowledge and appreciate receiving a copy of form PTO-1449, on which the examiner has initialed all listed items.

Claims 1 – 20 are pending. New claims 10 – 20 have been added. The applicants respectfully request reconsideration and allowance of this application in view of the above amendments and the following remarks.

Claims 1 – 9 were rejected under 35 USC 102(e) as being unpatentable over US Patent 6,745,320, Mitsuishi ("Mitsuishi"). The rejection is respectfully traversed for reasons including the following, which are provided by way of example. As described in the application, the invention is directed to solving the problem of compiling bit operation expressions for a RISC CPU, so that "a bit operation expression can be replaced by a condition judgement expression." (Specification 7, lines 17 – 18.) FIG. 7 illustrates an example of object code generated by a prior art compiler for the source code expression bit1 = bit2 & bit3. FIG. 3 illustrates an example of object code generated by one or more embodiments, as claimed, from the same source code expression.

According to the claims, e.g., claim 1 as amended, the invention is directed to a compiler. The object code includes code for an instruction for judging the value of a bit variable and an instruction for assigning a value to a bit variable. The source code includes a bit operational

expression that expresses a result value for a bit variable in accordance with a combination of respective values of bit variables.

The compiler includes a convertor, responsive to input source code, to generate object code. A right-side portion of the bit operational expression in said source code is expressed in the object code as a condition judgement expression that is in accordance with Boolean logic. The condition judgement expression provides a result that is "true" when the combination of respective values has a predetermined first Boolean logic relationship and a result that is "false" when the combination of respective values has a predetermined second Boolean logic relationship. Further, it is expressed as instructions in the object code that selectively assign a predetermined first binary value and a predetermined second binary value that is the inverse of the first binary value to a bit variable which holds a result of the bit operation expression, in accordance with whether a "true" or a "false" decision is obtained from the condition judgement expression. (E.g., claim 1; see also claims 4, 6, 8, and 10 – 12.) Thereby, the number of steps required to be executed by the CPU for portions of the source code which involve bit variables can be reduced, with a substantial increase in processing speed.

Without conceding that Mitsuishi discloses any feature of the present invention, Mitsuishi is directed to a data processing apparatus "capable of increasing a number of general purpose registers while maintaining upper compatibility" (Abstract). Mistuishi recognizes the problem of "register architecture, upper compatibility, and expression of operational function" (Col. 1, lines 9 – 13). According to the office action, the most relevant portions of Mitsuishi discuss that "the C compiler utilizes instruction designated by the usable combination of operation, data size and addressing mode, general purpose registers, address spaces, converts programs by C language into instruction of CPU and outputs it as assembly language programs or object modules." (Column 68, lines 21 - 27). Further, Mitsuishi states that "development efficiency can be

promoted." (Col. 68, lines 41 – 42.) Mitsuishi also acknowledges that bit operation instructions, e.g., bit test instructions exist.

The office action asserts that Mitsuishi discloses the invention as claimed. To the contrary, Mitsuishi fails to teach or suggest the invention, as presently claimed, when the claims are considered as a whole. Mitsuishi fails to teach or suggest, for example, "a right side portion of said bit operational expression in said source code being expressed in the object code as a condition judgement expression." Also, Mistuishi fails to teach or suggest "being expressed as instructions in the object code that selectively assign a predetermined first binary value and a predetermined second binary value ... in accordance with whether a "true" or a "false" decision is obtained from said condition judgement expression" (See, e.g., claim 1.) To the contrary, Mitsuishi does not teach or suggest anything about how a bit operation expression in source code expressions should be expressed in object code.

To anticipate a claim, a single reference must teach each and every element as set forth in the claim. *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). "The identical invention must be shown in as complete detail as is contained in the ... claim." *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989).

The Office Action argues that Mitsuishi teaches or suggests a bit test instruction and bit set instruction. However, the existence of specific bit instructions fails to teach or suggest how the source code should be compiled in order to generate such instructions. Consequently, Mistuishi fails to teach or suggest generating object code from input source code where a bit operation instruction in the source code is expressed as a condition judgment expression. (See, e.g., claim 1s, 4, 6, 8, and 10 – 12.)

Mitsuishi simply fails to teach or suggest, for example, the specific elements recited in independent claims 1, 4, 6, 8, and 10 – 12. It is respectfully submitted therefore that claims 1, 4, 6, 8, and 10 – 12 are patentable over Mitsuishi.

For at least these reasons, the combination of features recited in independent claims 1, 4, 6, 8, and 10 – 12, when interpreted as a whole, is submitted to patentably distinguish over the prior art. In addition, Mitsuishi clearly fails to show other claimed features as well.

With respect to the rejected dependent claims, applicant respectfully submits that these claims are allowable not only by virtue of their dependency from independent claims 1, 4, 6, 8, and 10 – 12, but also because of additional features they recite in combination.

New claims 10 – 20 have been added to further define the invention, and are believed to be patentable for reasons including these set out above.

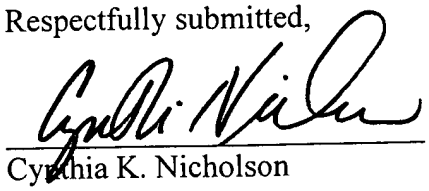
The applicants respectfully submit that, as described above, the cited prior art does not show or suggest the combination of features recited in the claims. The applicants do not concede that the cited prior art shown any of the elements recited in the claims. However, the applicants have provided specific examples of elements in the claims that are clearly not present in the cited prior art.

The applicants strongly emphasize that one reviewing the prosecution history should not interpret any of the examples the applicants have described herein in connection with distinguishing over the prior art as limiting to those specific features in isolation. Rather, for the sake of simplicity, the applicants have provided examples of why the claims described above are distinguishable over the cited prior art.

In view of the forgoing, the applicants respectfully submit that this application is in condition for allowance. A timely notice to that effect is respectfully requested. If questions relating to patentability remain, the examiner is invited to contact the undersigned by telephone.

Please charge any unforeseen fees that may be due to Deposit Account No. 50-1147.

Respectfully submitted,



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